(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
21 May 2004 (21.05.2004)

PCT

(10) International Publication Number
WO 2004/042920 A2

(51) International Patent Classification[7]: H03H 7/01

(21) International Application Number:
PCT/IB2003/004840

(22) International Filing Date: 30 October 2003 (30.10.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
02102553.1 8 November 2002 (08.11.2002) EP

(71) Applicant *(for all designated States except US)*: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: KWONG, Kam, Choon [MY/DE]; Philips Intellectual Property & Standards GmbH, Weisshausstr. 2, 52066 Aachen (DE).

(74) Agent: VOLMER, Georg; Philips Intellectual Property & Standards GmbH, Weisshausstr. 2, 52066 Aachen (DE).

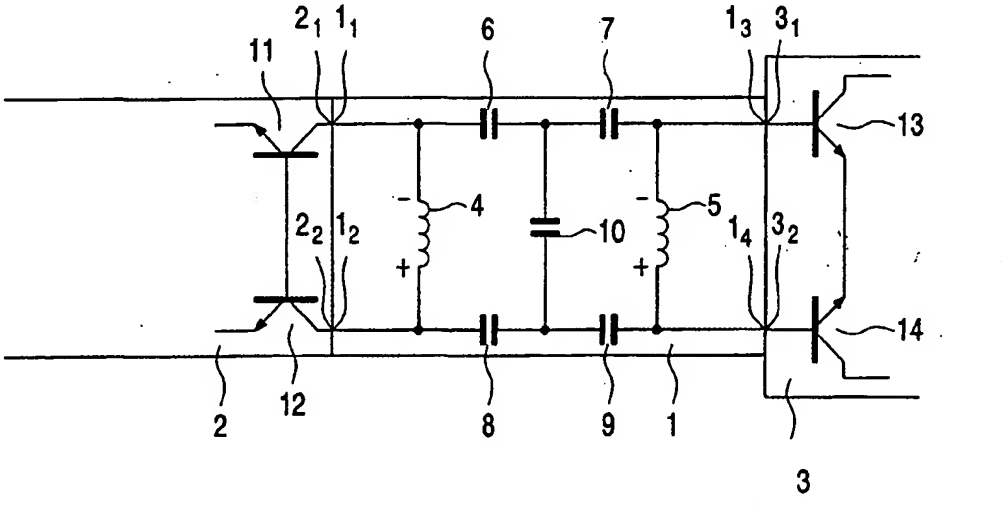
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: A FLAT INTERMEDIATE IF FILTER FOR TUNERS



(57) Abstract: The invention describes an intermediate frequency input circuit (1), which is coupled between output nodes of a frequency mixing circuit (2) and input nodes of an intermediate frequency amplifier circuit (3). The intermediate frequency circuit (1) comprises a first inductor (4), a first capacitor (6) and a third capacitor (8), which are in resonance with a lower intermediate frequency and a second inductor (5), a second capacitor (7), a fourth capacitor (8), which are in resonance with an upper intermediate frequency. These resonant frequencies are coupled by a fifth capacitor (10) in order to obtain a flat graph of a frequency characteristic of the intermediate frequency input circuit 1.

WO 2004/042920 A2

A flat intermediate IF filter for tuners

The present invention relates to an intermediate frequency input circuit, which is coupled between output nodes of a frequency mixing circuit and input nodes of an intermediate frequency amplifier circuit.

In some television tuners, an intermediate frequency input circuit is connected between output ends of a frequency mixing circuit and input ends of an intermediate frequency amplifier circuit. The intermediate frequency circuit allows a selective intermediate frequency signal of a selector channel to pass while rejecting undesired frequency components that may occur near the intermediate frequency. A rejected frequency component may include an intermediate frequency component of an upper adjacent channel and an intermediate frequency component of a lower adjacent channel. Accordingly, undesired frequency components are not received by the intermediate frequency amplifier circuit.

In the future analog and digital signals are expected to coexist before the full switch to digital signals will be realized. Since the digital transmission is usually reduced in power, the protection from strong adjacent analog channels becomes more critical.

It is, inter alia, an object of the present invention to provide an intermediate frequency input circuit having a flat frequency response for an intermediate frequency of a selector channel and providing sufficient suppression of adjacent channels.

The present invention solves the described problem by providing an intermediate frequency input circuit, which is connected between output nodes of a frequency mixing circuit and input nodes of an intermediate frequency amplifier circuit. The intermediate frequency input circuit includes a pair of input nodes and a pair of output nodes, a first inductor being coupled between the pair of input nodes and

a second inductor being coupled between the pair of input nodes, a first and a second capacitor, which are coupled between a first input node and a first output node,

a third and a fourth capacitor, which are coupled between a second input node and a second output node and a fifth capacitor, which is coupled between the first capacitor and the fourth capacitor and between the second capacitor and the third capacitor.

Compared with a characteristic of a known intermediate frequency input circuit with this arrangement a flat frequency response over a few MHz for the intermediate frequency of the selector channel is obtained. Additionally a satisfactory trap characteristics for the intermediate frequency component of the upper adjacent channel and for the intermediate frequency component of the lower adjacent channel. The intermediate frequency input circuit is cost effective and gives a flat response with good suppression of the sound and adjacent channels without using traps, which usually need to be aligned during production.

Fig. 1 shows, in a schematic diagram, an embodiment of an intermediate frequency input circuit; and

Fig. 2 is a graph showing an example of a frequency characteristic of the intermediate frequency input circuit shown in Fig. 1.

The present invention is illustrated from the following description of the preferred embodiment and the accompanying drawings.

Fig.1 shows an embodiment of an intermediate frequency input circuit 1. The intermediate frequency input circuit 1 is coupled between a frequency mixing circuit 2 and an intermediate frequency amplifier circuit 3.

The intermediate frequency input circuit 1 includes a pair of input nodes 1_1 and 1_2, a pair of output nodes 1_3 and 1_4, a first inductor 4, a second inductor 5, a first and a second capacitor 6 and 7, a third and a fourth capacitor 8 and 9, and a fifth capacitor 10.

The frequency mixing circuit 2 includes a pair of input nodes 2_1 and 2_2 a pair of output transistors 11 and 12 in a common-base configuration.

The intermediate frequency amplifier circuit 3 includes a pair of input nodes 3_1 and 3_2 and a pair of input transistors 13 and 14 in a common-emitter configuration.

In the intermediate frequency input circuit 1, the first inductor 4 is coupled between the pair of input nodes 1_1 and 1_2. Between one input node 1_1 and one output node 1_3 the first capacitor 6 and the second capacitor 7 are coupled in series, whereby the first

capacitor is coupled to input node 1_1 and to the second capacitor 7. The second capacitor 7 is coupled to the output node 1_3. The second inductor 5 is coupled between the pair of output nodes 1_3 and 1_4. Between one input node 1_2 and one output node 1_4 the third capacitor 8 and the second capacitor 9 are coupled in series, whereby the third capacitor is coupled to input node 1_2 and to the fourth capacitor 9. The fourth capacitor 9 is also coupled to the output node 1_4.

In the frequency mixing circuit 2 a collector of one output transistor 11 is coupled to one output node 2_1, and a collector of the other output transistor 12 is coupled to the other output node 2_2.

In the intermediate frequency amplifier circuit 3 a base of one input transistor 13 is coupled to one input node 3_1, and a base of the other input transistor 14 is coupled to the other input node 3_2.

The pair of input nodes 1_1 and 1_2 of the intermediate frequency input circuit 1 is coupled to the pair of output nodes 2_1 and 2_2 of the frequency mixing circuit 2. The pair of output nodes 1_3 and 1_4 of the intermediate frequency input circuit 1 is coupled to the pair of input nodes 3_1 and 3_2 of the intermediate frequency amplifier circuit 3.

In the preferred intermediate frequency the input circuit 1, the inductance of the first inductor 4 and the capacitance of the first and third capacitors 6 and 8 are selected so that the first inductor 4 and the first and third capacitors 6 and 8 are in resonance with a lower intermediate frequency of the selector channel. The inductance of the second inductor 5 and the capacitance of the second and fourth capacitors 7 and 9 are selected so that the second inductor 5 and the second and fourth capacitors 7 and 9 are in resonance with an upper intermediate frequency of the selector channel. By coupling the component of the lower resonant frequency and the upper resonant frequency with the fifth capacitor 10 a flat frequency response over a few MHz of the intermediate frequency input circuit 1 can be obtained.

The intermediate frequency input circuit 1 operates as follows. An intermediate frequency signal (hereinafter referred to as an "IF signal") of the selector channel passes through the pair of output nodes 2_1 and 2_2 of the frequency mixing circuit 2. The IF signal includes undesired frequency components. It is received by the intermediate frequency input circuit 1 through the pair of input nodes 1_1 and 1_2. The first inductor 4 and the first and third capacitors 6 and 8 select lower intermediate frequencies of the selector channel. The second inductor 5 and the second and fourth capacitors 7 and 9 select upper intermediate frequency of the selector channel. The adjusted IF signal is passed through the

pair of output nodes 1_3 and 1_4 and is received by the pair of input nodes 3_1 and 3_2 of the intermediate frequency amplifier circuit 3. The IF signal is then preferably amplified by the pair of input transistors 13 and 14.

Fig. 2 shows an example of a frequency characteristic of the intermediate frequency input circuit shown in Fig. 1. The inductance of the first inductor 4 and the capacitance of the first and third capacitors 6 and 8 are selected so that the lower resonant frequency is 34.47 MHz and the inductance of the second inductor 5 and the capacitance of the second and fourth capacitors 7 and 9 are selected so that the upper resonant frequency is 38.9 MHz. The bandwidth of the intermediate frequency input circuit is adjusted by the fifth capacitor 10.

CLAIMS:

1. An intermediate frequency circuit (1), which is connected between a frequency mixing circuit (2) and an intermediate frequency amplifier circuit (3), the intermediate frequency circuit (1) comprising:

a pair of input nodes(1_1, 1_2);

a pair of output nodes (1_3, 1_4);

a first inductor (4) being coupled between the pair of input nodes (1_1, 1_2);

a second inductor (5) being coupled between the pair of output nodes (1_3, 1_4);

a first and a second capacitor (6, 7), which are coupled between a first input node (1_1) and a first output node (1_3);

a third and a fourth capacitor (8, 9), which are coupled between a second input node (1_2) and a second output node (1_4); and

a fifth capacitor (10), which is coupled between the first capacitor (6) and the fourth capacitor (8) and between the second capacitor (7) and the third capacitor (8).

2. The intermediate frequency circuit of claim 1, wherein said first capacitor (6) is coupled in series to said second capacitor (7); and

said third capacitor (8) is coupled in series to said fourth capacitor (9).

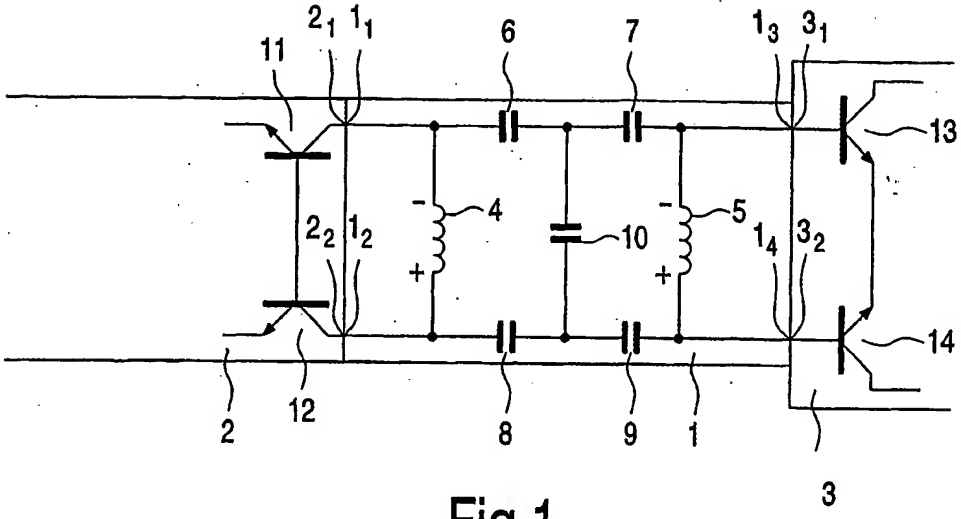

2_1 1_1
11
6
7
1_3 3_1
13
4
5
10
2_2 1_2
1_4 3_2
14
2
12
8
9
1
3

Fig.1

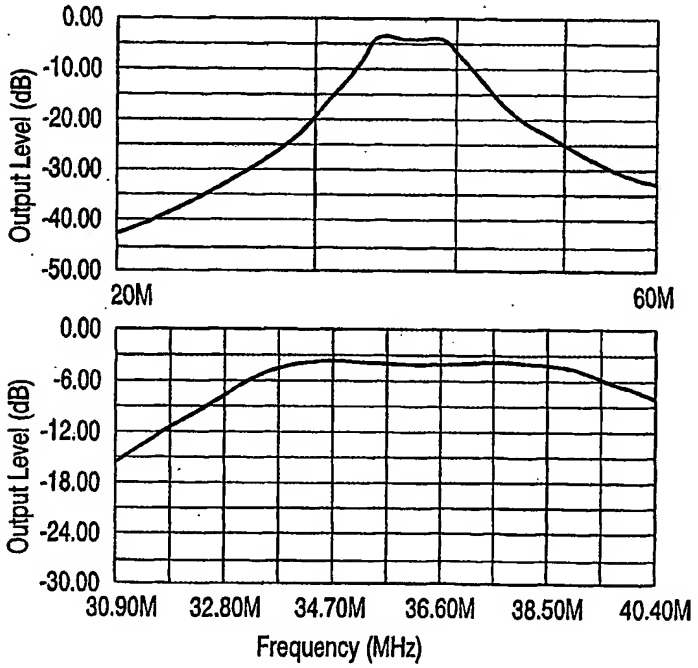

0.00
-10.00
-20.00
-30.00
-40.00
-50.00
Output Level (dB)
20M
60M
0.00
-6.00
-12.00
-18.00
-24.00
-30.00
Output Level (dB)
30.90M
32.80M
34.70M
36.60M
38.50M
40.40M
Frequency (MHz)

Fig.2

INTERNATIONAL SEARCH REPORT

Ir onal Application No
PCT/IB 03/04840

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03H7/01 H03H7/01

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	BE 389 750 A (NV PHILIPS GLOEILAMPFABRIEKEN) 31 August 1932 (1932-08-31) page 2, line 26 - page 3, line 15; figure 1	1,2
P,X	US 2003/124996 A1 (AMIOT SEBASTIEN ET AL) 3 July 2003 (2003-07-03) paragraph '0036! - paragraph '0042!; figures 3,6	1,2

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 May 2004	04/08/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Lecoutre, R

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/IB 03/04840

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
BE 389750 A		NONE	
US 2003124996 A1	03-07-2003	FR 2832874 A1	30-05-2003
		CN 1421995 A	04-06-2003
		EP 1315295 A1	28-05-2003
		JP 2003168993 A	13-06-2003